SPECIFICATION

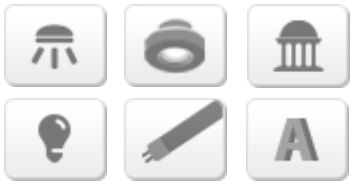
Product : STW8A12D-T2-W

Seoul Semiconductor			Customer
Drawn by	Checked by	Approved by	Approved by
J.M.Lee		Z.H.Lee	

Mid-Power LED – 3528 T Series

STW8A12D-T2-W

(Cool, Neutral, Warm)



LM-80

RoHS

Product Brief

Description

- This White Colored surface-mount LED comes in standard package dimension.
- It has a substrate made up of a molded plastic reflector sitting on top of a lead frame.
- The die is attached within the reflector cavity and the cavity is encapsulated by silicone.
- The package design coupled with careful selection of component materials allow these products to perform with high reliability.

Features and Benefits

- Market Standard 3528 Package Size
- Competitive performance and cost
- Coating Technology to Improve Reliability
- RoHS compliant
- Package Size: 3.5x2.8

Key Applications

- Interior lighting
- General lighting
- Indoor displays
- Architectural / Decorative lighting

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Product Performance & Characterization Guide

Table 1. Product Selection Guide, I_F = 150mA, T_j = 25ºC, RH30%

CRI min	CCT	Performance	Flux & Lm/w(typ) I_F=150mA, T1 VF_{typ}=3.16V
			8T2
80	6500K	Flux	62
		lm/w	130
	5700K	Flux	62.5
		lm/w	131
	5000K	Flux	63
		lm/w	132
	4000K	Flux	62
		lm/w	130
	3500K	Flux	59.5
		lm/w	125
	3000K	Flux	58.5
		lm/w	123
	2700K	Flux	56.5
		lm/w	119

Notes :

(1) Correlated Color Temperature is derived from the CIE 1931 Chromaticity diagram.

(2) Seoul Semiconductor maintains a tolerance of ±5% on Flux and power measurements. The luminous Flux was measured at the peak of the spatial pattern which may not be aligned with the mechanical axis of the LED package.

Product Performance & Characterization Guide

Table 2. Characteristics, I_F=150mA, T_j=25ºC

Parameter	Symbol	Bin	Value			Unit
			Min.	Typ.	Max.	
Forward Voltage	V_F	Y2	2.80		2.90	V
		Y3	2.90		3.00	
		Z1	3.00		3.10	
		Z2	3.10	-	3.20	
		Z3	3.20		3.30	
Forward Current	I_F		-	150	-	mA
CRI [3]	R_a	-	80	82	-	
			90	92	-	
Viewing Angle	$2\Theta_{1/2}$		-	120	-	Deg.
Thermal resistance (J to S) [4]	$R\theta_{J\text{-}S}$		-	15	-	℃/W
ESD Sensitivity(HBM)	-		Class 2 JESD22-A114-E			

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Forward Current	I_F	180	mA
Junction Temperature	T_j	115	ºC
Operating Temperature	T_{opr}	-40 ~ + 85	ºC
Storage Temperature	T_{stg}	-40 ~ + 100	ºC

Notes :

(1) Seoul Semiconductor maintains a tolerance of ±5% on Flux and power measurements.

(2) Correlated Color Temperature is derived from the CIE 1931 Chromaticity diagram.

Color coordinate : ±0.005, CCT ±5% tolerance.

(3) Tolerance is ±2.0 on CRI,±0.1V on VF measurements.

(4) Thermal resistance is junction to Solder.

(5) The products are sensitive to static electricity and must be carefully taken when handling products

(6) It is recommended minimum currrent 5mA in order to avoid unstable brightness, and may vary depending on circuit configuration

(7) It is recommended to use it in the condition that the reliability is secured within the Max value.

- **Calculated performance values are for reference only.**
- **All measurements were made under the standardized environment of Seoul Semiconductor.**

Characteristics Graph

Fig 1. Color Spectrum, T_j = 25ºC, I_F=150mA

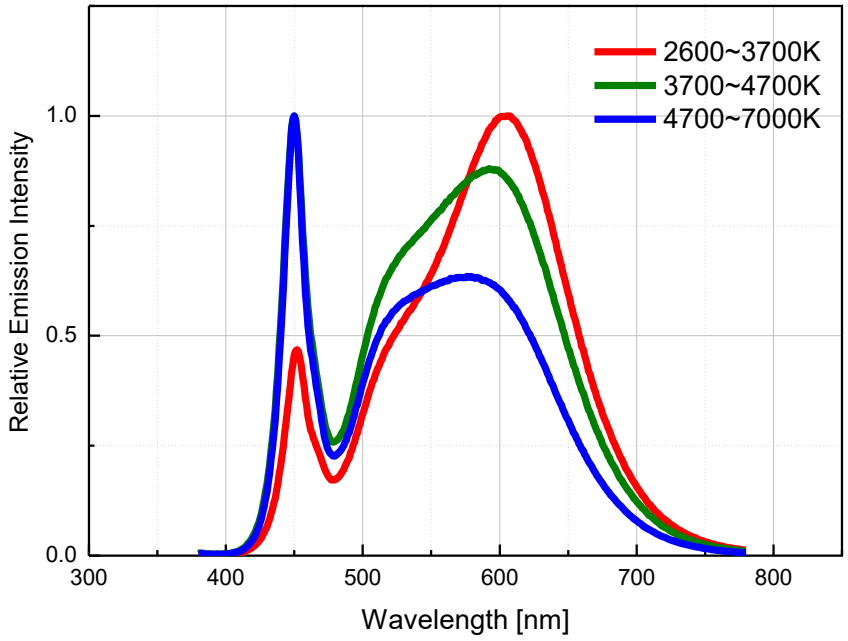
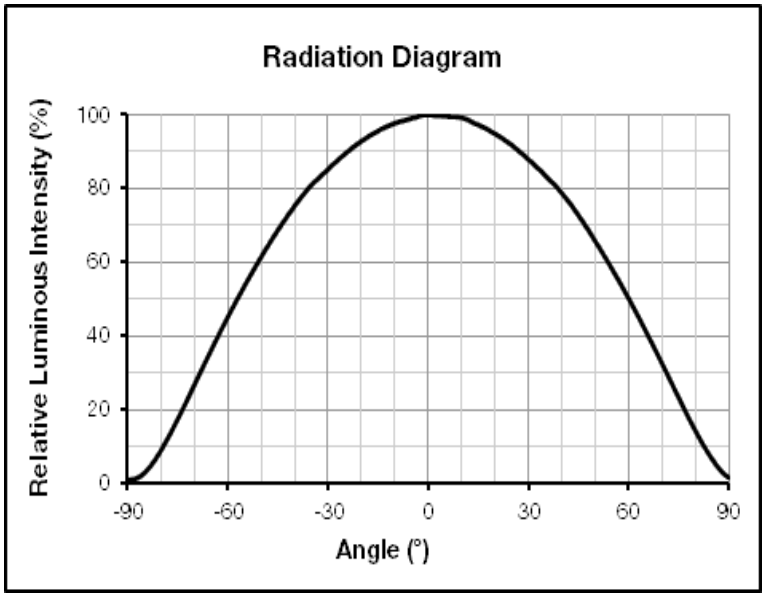


Fig 2. Radiant Pattern, T_j = 25ºC, I_F=150mA



Characteristics Graph

Fig 3. Forward Voltage vs. Forward Current, T_j = 25ºC

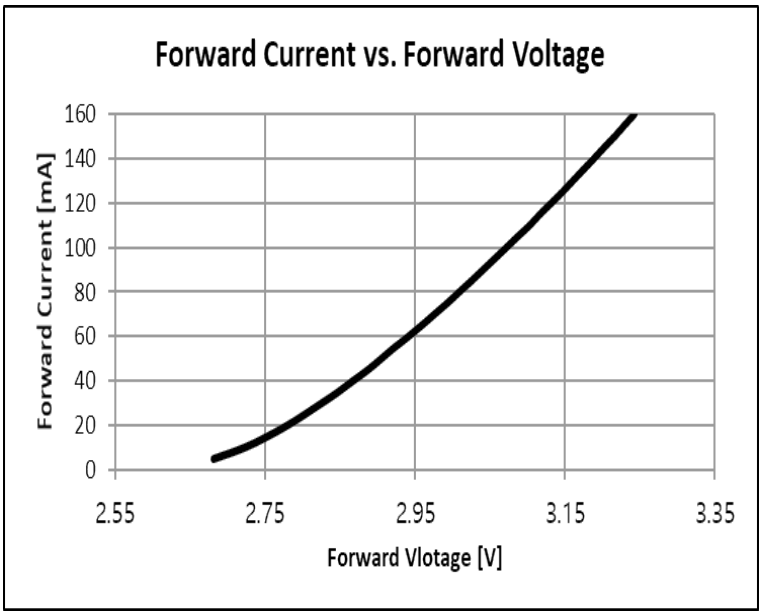
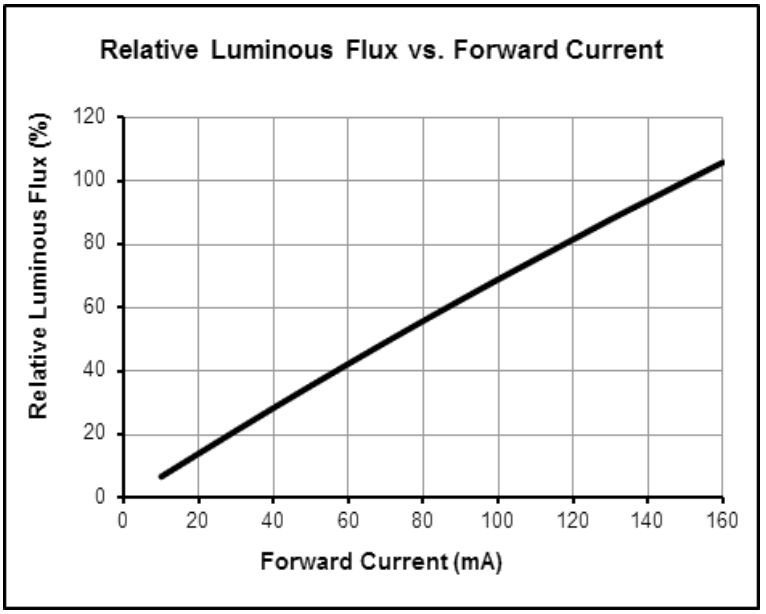
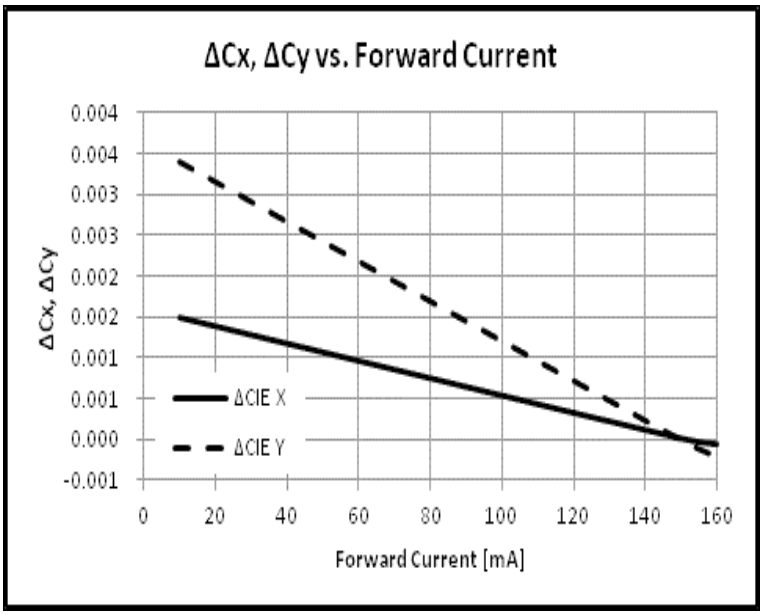


Fig 4. Forward Current vs. Relative Luminous Flux, T_j = 25ºC



Characteristics Graph

Fig 5. Forward Current vs. CIE X,Y Shift, T_j = 25ºC



Characteristics Graph

Fig 6. Junction Temperature vs. Relative Luminous Flux, I_F=150mA

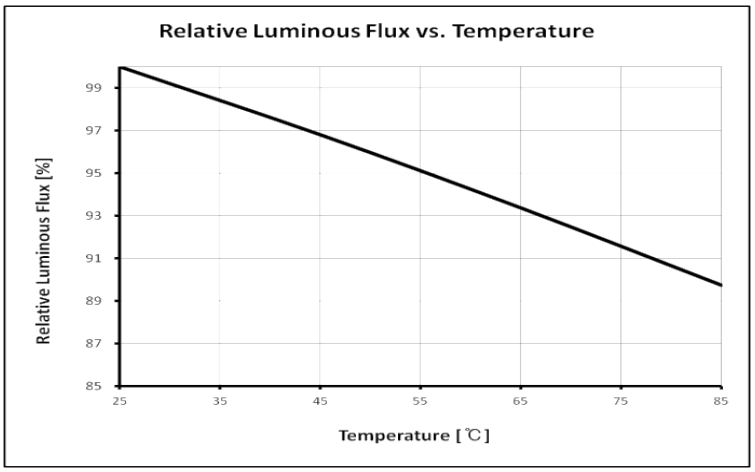
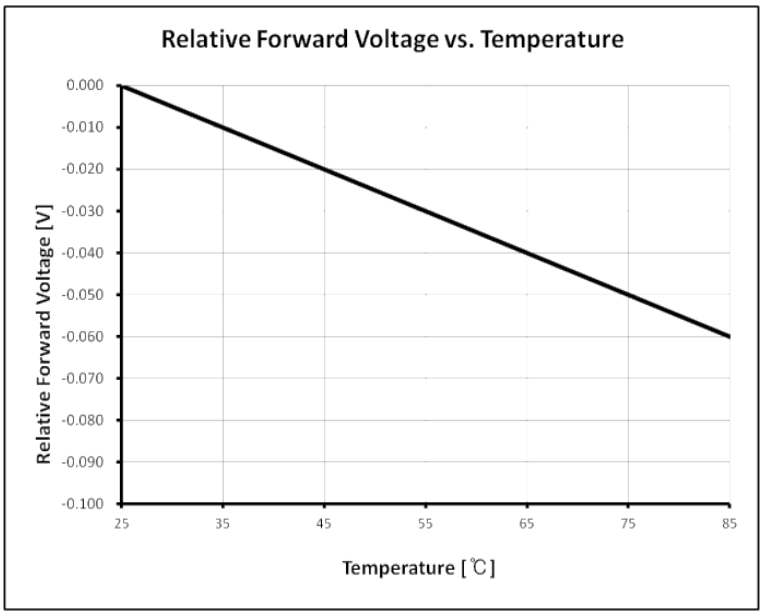


Fig 7. Junction Temperature vs. Relative Forward Voltage, I_F=150mA



Characteristics Graph

Fig 8. Chromaticity Coordinate vs. Junction Temperature, I_F=150mA

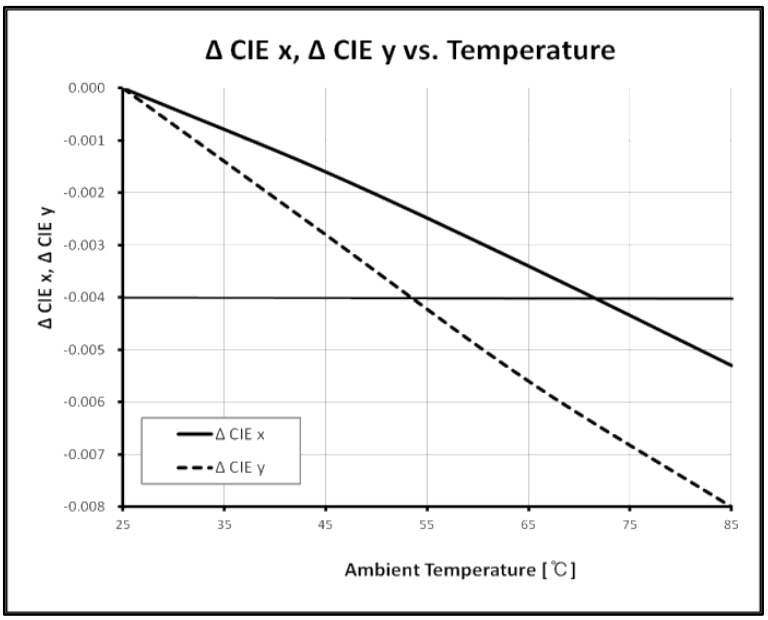
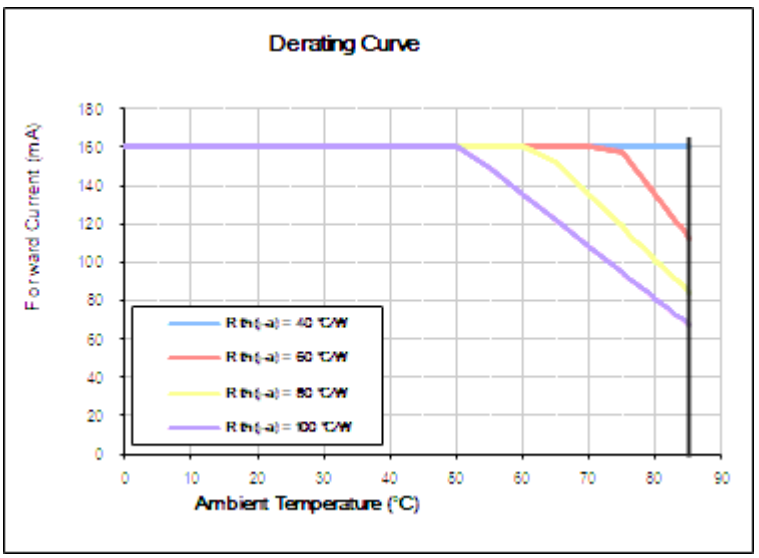


Fig 9. Ambient Temperature vs. Maximum Forward Current, T_{j_max} = 125℃



Color Bin Structure

Table 4. Available Flux Rank ,T_j=25℃, I_F=150mA

CRI	Flux Bin	8T2	
	CCT	min	max
80	6500K	60	64
	5700K	60.5	64.5
	5000K	61	65
	4000K	60	64
	3500K	57.5	61.5
	3000K	56.5	60.5
	2700K	54.5	58.5

Table 5. Available VF Rank ,T_j=25℃, I_F=150mA

Item	Unit	Bin Code	Min.	Max.
Forward Voltage (VF)	V	Y2	2.80	2.90
		Y3	2.90	3.00
		Z1	3.00	3.10
		Z2	3.10	3.20
		Z3	3.20	3.30

- All measurements were made under the standardized environment of Seoul Semiconductor.
- Typ value is according to 4000K

Color Bin Structure

Kitting rule

- 1) Kitting bin Concept
- 1.Under agreement between customer and Seoul Semiconductor., Seoul can supply kitting bin (VF, Color, lm).
- 2.A forward voltage (VF) of kitting bin is combined by a pair of same VF rank such as (Y2+Y2), (Y3+Y3), (Z1+Z1), (Z2+Z2) or (Z3+Z3).
- 3.A Chromaticity Coordinates of kitting bin is mixed by kitting procedure.(below kitting simulation)

[Kitting example]

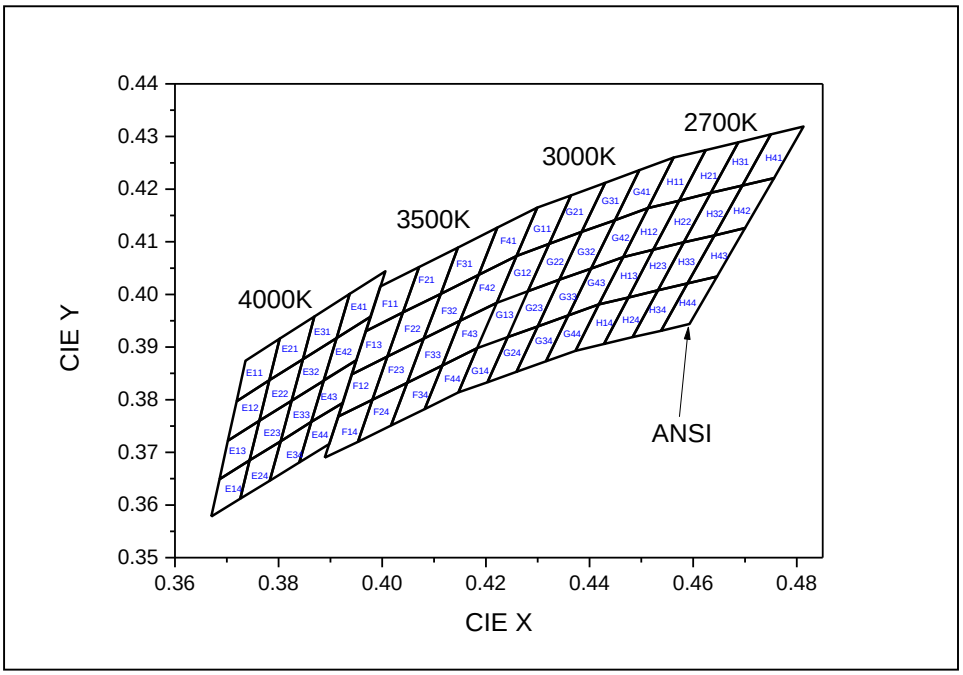
11	21	31	41
12	22	32	42
13	23	33	43
14	24	34	44

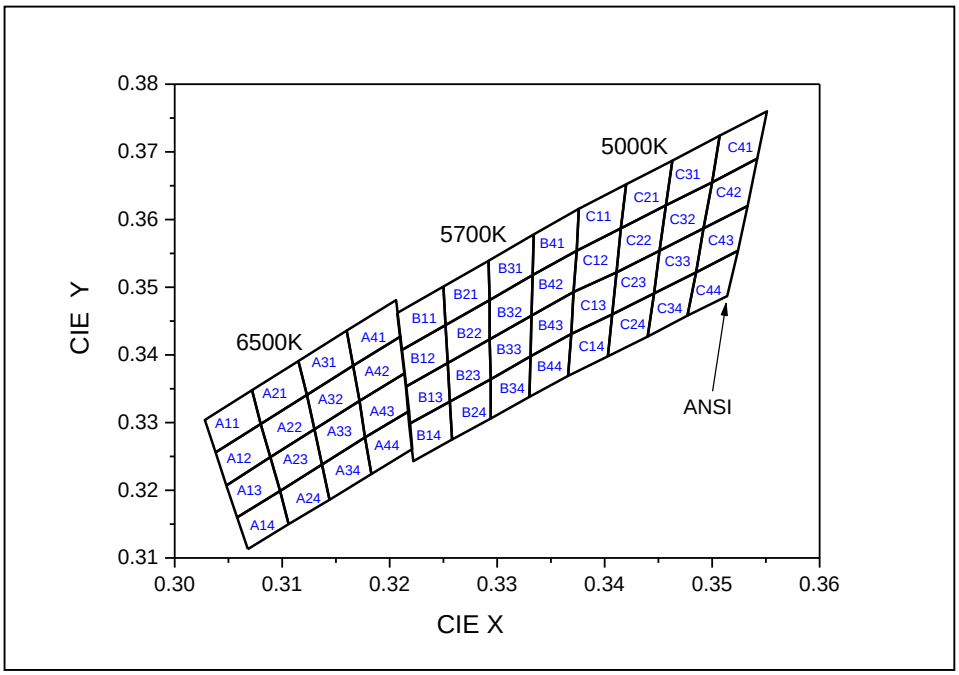
[Binning Information]

	Bin #1	Bin #2
VF	Y2	Y2
	Y3	Y3
	Z1	Z1
	Z2	Z2
	Z3	Z3
CIE	14, 24, 13 bin	42, 31, 41 bin
	23, 33, 22, 32 bin	23, 33, 22, 32 bin
	34, 44, 43 bin	12, 11, 21 bin
	14, 24, 13 bin	42, 31, 41 bin

Color Bin Structure

CIE Chromaticity Diagram T_a=25℃, I_F=150mA





***Notes :**

1. H=2700K G=3000K F=3500K E=4000K C=5000K B=5700K A=6500K

Color Bin Structure

Chromaticity Region & Coordinates

Region	CIE x	CIE y	Region	CIE x	CIE y
Hrank(2700K)					
H14	0.4373	0.3893	H12	0.4465	0.4071
	0.4418	0.3981		0.4513	0.4164
	0.4475	0.3994		0.4573	0.4178
	0.4428	0.3906		0.4523	0.4085
H24	0.4428	0.3906	H22	0.4523	0.4085
	0.4475	0.3994		0.4573	0.4178
	0.4532	0.4008		0.4634	0.4193
	0.4483	0.3919		0.4582	0.4099
H34	0.4483	0.3919	H32	0.4582	0.4099
	0.4532	0.4008		0.4634	0.4193
	0.4589	0.4021		0.4695	0.4207
	0.4538	0.3931		0.4641	0.4112
H44	0.4538	0.3931	H42	0.4641	0.4112
	0.4589	0.4021		0.4695	0.4207
	0.4646	0.4034		0.4756	0.4221
	0.4593	0.3944		0.4700	0.4126
H13	0.4418	0.3981	H11	0.4513	0.4164
	0.4465	0.4071		0.4562	0.4260
	0.4523	0.4085		0.4624	0.4274
	0.4475	0.3994		0.4573	0.4178
H23	0.4475	0.3994	H21	0.4573	0.4178
	0.4523	0.4085		0.4624	0.4274
	0.4582	0.4099		0.4687	0.4289
	0.4532	0.4008		0.4634	0.4193
H33	0.4532	0.4008	H31	0.4634	0.4193
	0.4582	0.4099		0.4687	0.4289
	0.4641	0.4112		0.4750	0.4304
	0.4589	0.4021		0.4695	0.4207
H43	0.4589	0.4021	H41	0.4695	0.4207
	0.4641	0.4112		0.4750	0.4304
	0.4700	0.4126		0.4813	0.4319
	0.4646	0.4034		0.4756	0.4221

Region	CIE x	CIE y	Region	CIE x	CIE y
Grank(3000K)					
G14	0.4147	0.3814	G12	0.4221	0.3984
	0.4183	0.3898		0.4259	0.4073
	0.4242	0.3919		0.4322	0.4096
	0.4203	0.3833		0.4281	0.4006
G24	0.4203	0.3833	G22	0.4281	0.4006
	0.4242	0.3919		0.4322	0.4096
	0.4300	0.3939		0.4385	0.4119
	0.4259	0.3853		0.4342	0.4028
G34	0.4259	0.3853	G32	0.4342	0.4028
	0.4300	0.3939		0.4385	0.4119
	0.4359	0.3960		0.4449	0.4141
	0.4316	0.3873		0.4403	0.4049
G44	0.4316	0.3873	G42	0.4403	0.4049
	0.4359	0.3960		0.4449	0.4141
	0.4418	0.3981		0.4513	0.4164
	0.4373	0.3893		0.4465	0.4071
G13	0.4183	0.3898	G11	0.4259	0.4073
	0.4221	0.3984		0.4299	0.4165
	0.4281	0.4006		0.4364	0.4188
	0.4242	0.3919		0.4322	0.4096
G23	0.4242	0.3919	G21	0.4322	0.4096
	0.4281	0.4006		0.4364	0.4188
	0.4342	0.4028		0.4430	0.4212
	0.4300	0.3939		0.4385	0.4119
G33	0.4300	0.3939	G31	0.4385	0.4119
	0.4342	0.4028		0.4430	0.4212
	0.4403	0.4049		0.4496	0.4236
	0.4359	0.3960		0.4449	0.4141
G43	0.4359	0.3960	G41	0.4449	0.4141
	0.4403	0.4049		0.4496	0.4236
	0.4465	0.4071		0.4562	0.4260
	0.4418	0.3981		0.4513	0.4164

Note: Seoul Semiconductor maintains measurement tolerance of: Cx, Cy = ±0.005

Color Bin Structure

Chromaticity Region & Coordinates

Region	CIE x	CIE y	Region	CIE x	CIE y
Frank(3500K)					
F14	0.3889	0.3690	F12	0.3941	0.3848
	0.3915	0.3768		0.3968	0.3930
	0.3981	0.3800		0.4040	0.3966
	0.3953	0.3720		0.4010	0.3882
F24	0.3953	0.3720	F22	0.4010	0.3882
	0.3981	0.3800		0.4040	0.3966
	0.4048	0.3832		0.4113	0.4001
	0.4017	0.3751		0.4080	0.3916
F34	0.4017	0.3751	F32	0.4080	0.3916
	0.4048	0.3832		0.4113	0.4001
	0.4116	0.3865		0.4186	0.4037
	0.4082	0.3782		0.4150	0.3950
F44	0.4082	0.3782	F42	0.4150	0.3950
	0.4116	0.3865		0.4186	0.4037
	0.4183	0.3898		0.4259	0.4073
	0.4147	0.3814		0.4221	0.3984
F13	0.3915	0.3768	F11	0.3968	0.3930
	0.3941	0.3848		0.3996	0.4015
	0.4010	0.3882		0.4071	0.4052
	0.3981	0.3800		0.4040	0.3966
F23	0.3981	0.3800	F21	0.4040	0.3966
	0.4010	0.3882		0.4071	0.4052
	0.4080	0.3916		0.4146	0.4089
	0.4048	0.3832		0.4113	0.4001
F33	0.4048	0.3832	F31	0.4113	0.4001
	0.4080	0.3916		0.4146	0.4089
	0.4150	0.3950		0.4222	0.4127
	0.4116	0.3865		0.4186	0.4037
F43	0.4116	0.3865	F41	0.4186	0.4037
	0.4150	0.3950		0.4222	0.4127
	0.4221	0.3984		0.4299	0.4165
	0.4183	0.3898		0.4259	0.4073

Region	CIE x	CIE y	Region	CIE x	CIE y
Erank (4000K)					
E14	0.3670	0.3578	E12	0.3702	0.3722
	0.3726	0.3612		0.3763	0.3760
	0.3744	0.3685		0.3782	0.3837
	0.3686	0.3649		0.3719	0.3797
E24	0.3726	0.3612	E22	0.3763	0.3760
	0.3783	0.3646		0.3825	0.3798
	0.3804	0.3721		0.3847	0.3877
	0.3744	0.3685		0.3782	0.3837
E34	0.3783	0.3646	E32	0.3825	0.3798
	0.3840	0.3681		0.3887	0.3836
	0.3863	0.3758		0.3912	0.3917
	0.3804	0.3721		0.3847	0.3877
E44	0.3840	0.3681	E42	0.3887	0.3837
	0.3898	0.3716		0.3950	0.3875
	0.3924	0.3794		0.3978	0.3958
	0.3863	0.3758		0.3912	0.3917
E13	0.3686	0.3649	E11	0.3719	0.3797
	0.3744	0.3685		0.3782	0.3837
	0.3763	0.3760		0.3802	0.3916
	0.3702	0.3722		0.3736	0.3874
E23	0.3744	0.3685	E21	0.3782	0.3837
	0.3804	0.3721		0.3847	0.3877
	0.3825	0.3798		0.3869	0.3958
	0.3763	0.3760		0.3802	0.3916
E33	0.3804	0.3721	E31	0.3847	0.3877
	0.3863	0.3758		0.3912	0.3917
	0.3887	0.3836		0.3937	0.4001
	0.3825	0.3798		0.3869	0.3958
E43	0.3863	0.3758	E41	0.3912	0.3917
	0.3924	0.3794		0.3978	0.3958
	0.3950	0.3875		0.4006	0.4044
	0.3887	0.3836		0.3937	0.4001

Note: Seoul Semiconductor maintains measurement tolerance of: Cx, Cy = ±0.005

Color Bin Structure

Chromaticity Region & Coordinates

Region	CIE x	CIE y	Region	CIE x	CIE y	Region	CIE x	CIE y	Region	CIE x	CIE y
Crank(5000K)						Brank (5700K)					
C14	0.3366	0.3369	C12	0.3374	0.3554	B14	0.3218	0.3298	B12	0.3211	0.3407
	0.3369	0.3431		0.3371	0.3493		0.3222	0.3243		0.3215	0.3353
	0.3407	0.3460		0.3411	0.3522		0.3258	0.3275		0.3254	0.3388
	0.3403	0.3398		0.3415	0.3587		0.3256	0.3331		0.3252	0.3444
C24	0.3403	0.3398	C22	0.3415	0.3587	B24	0.3256	0.3331	B22	0.3252	0.3444
	0.3407	0.3460		0.3411	0.3522		0.3258	0.3275		0.3254	0.3388
	0.3446	0.3491		0.3451	0.3554		0.3294	0.3306		0.3293	0.3423
	0.3440	0.3427		0.3457	0.3621		0.3294	0.3364		0.3293	0.3481
C34	0.3446	0.3491	C32	0.3451	0.3554	B34	0.3294	0.3364	B32	0.3293	0.3481
	0.3440	0.3427		0.3457	0.3621		0.3294	0.3306		0.3293	0.3423
	0.3477	0.3458		0.3500	0.3655		0.3330	0.3338		0.3332	0.3458
	0.3485	0.3522		0.3492	0.3587		0.3331	0.3398		0.3333	0.3518
C44	0.3485	0.3522	C42	0.3492	0.3587	B44	0.3331	0.3398	B42	0.3333	0.3518
	0.3477	0.3458		0.3500	0.3655		0.3330	0.3338		0.3332	0.3458
	0.3514	0.3487		0.3542	0.3690		0.3366	0.3369		0.3371	0.3493
	0.3524	0.3554		0.3533	0.3620		0.3369	0.3431		0.3374	0.3554
C13	0.3371	0.3493	C11	0.3376	0.3616	B13	0.3215	0.3353	B11	0.3207	0.3462
	0.3369	0.3431		0.3374	0.3554		0.3218	0.3298		0.3211	0.3407
	0.3407	0.3460		0.3415	0.3587		0.3256	0.3331		0.3252	0.3444
	0.3411	0.3522		0.3420	0.3652		0.3254	0.3388		0.3250	0.3501
C23	0.3407	0.3460	C21	0.3415	0.3587	B23	0.3254	0.3388	B21	0.3250	0.3501
	0.3411	0.3522		0.3420	0.3652		0.3256	0.3331		0.3252	0.3444
	0.3451	0.3554		0.3463	0.3687		0.3294	0.3364		0.3293	0.3481
	0.3446	0.3491		0.3457	0.3621		0.3293	0.3423		0.3292	0.3539
C33	0.3446	0.3491	C31	0.3457	0.3621	B33	0.3293	0.3423	B31	0.3292	0.3539
	0.3451	0.3554		0.3463	0.3687		0.3294	0.3364		0.3293	0.3481
	0.3492	0.3587		0.3507	0.3724		0.3331	0.3398		0.3333	0.3518
	0.3485	0.3522		0.3500	0.3655		0.3332	0.3458		0.3334	0.3578
C43	0.3485	0.3522	C41	0.3500	0.3655	B43	0.3332	0.3458	B41	0.3334	0.3578
	0.3492	0.3587		0.3507	0.3724		0.3331	0.3398		0.3333	0.3518
	0.3533	0.3620		0.3551	0.3760		0.3369	0.3431		0.3374	0.3554
	0.3524	0.3554		0.3542	0.3690		0.3371	0.3493		0.3376	0.3616

Note: Seoul Semiconductor maintains measurement tolerance of: Cx, Cy = ±0.005

Color Bin Structure

Chromaticity Region & Coordinates

Region	CIE x	CIE y	Region	CIE x	CIE y
Arank(6500K)					
A14	0.3068	0.3113	A12	0.3048	0.3207
	0.3106	0.3150		0.3089	0.3249
	0.3098	0.3199		0.3080	0.3298
	0.3058	0.3160		0.3038	0.3256
A24	0.3106	0.3150	A22	0.3089	0.3249
	0.3144	0.3186		0.313	0.3290
	0.3137	0.3238		0.3123	0.3341
	0.3098	0.3199		0.3080	0.3298
A34	0.3144	0.3186	A32	0.3130	0.3290
	0.3183	0.3224		0.3172	0.3332
	0.3177	0.3278		0.3166	0.3384
	0.3137	0.3238		0.3123	0.3341
A44	0.3183	0.3224	A42	0.3172	0.3332
	0.3221	0.3261		0.3214	0.3373
	0.3218	0.3317		0.3210	0.3427
	0.3177	0.3278		0.3166	0.3384
A13	0.3058	0.3160	A11	0.3038	0.3256
	0.3098	0.3199		0.3080	0.3298
	0.3089	0.3249		0.3072	0.3348
	0.3048	0.3207		0.3028	0.3304
A23	0.3098	0.3199	A21	0.3080	0.3298
	0.3137	0.3238		0.3123	0.3341
	0.3130	0.3290		0.3115	0.3391
	0.3089	0.3249		0.3072	0.3348
A33	0.3137	0.3238	A31	0.3123	0.3341
	0.3177	0.3278		0.3166	0.3384
	0.3172	0.3332		0.3160	0.3436
	0.313	0.3290		0.3115	0.3391
A43	0.3177	0.3278	A41	0.3166	0.3384
	0.3218	0.3317		0.3210	0.3427
	0.3214	0.3373		0.3206	0.3481
	0.3172	0.3332		0.3160	0.3436

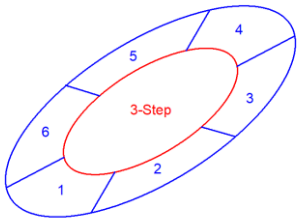
Note: Seoul Semiconductor maintains measurement tolerance of: Cx, Cy = ±0.005

Color Bin Structure

Kitting rule

- 1) Kitting bin Concept
- 1.Under agreement between customer and Seoul Semiconductor., Seoul can supply kitting bin (VF, Color, lm).
- 2.A forward voltage (VF) of kitting bin is combined by a pair of same VF rank such as (Y2+Y2), (Y3+Y3), (Z1+Z1), (Z2+Z2) or (Z3+Z3).
- 3.A Chromaticity Coordinates of kitting bin is mixed by kitting procedure.(below kitting simulation)

[Kitting example]

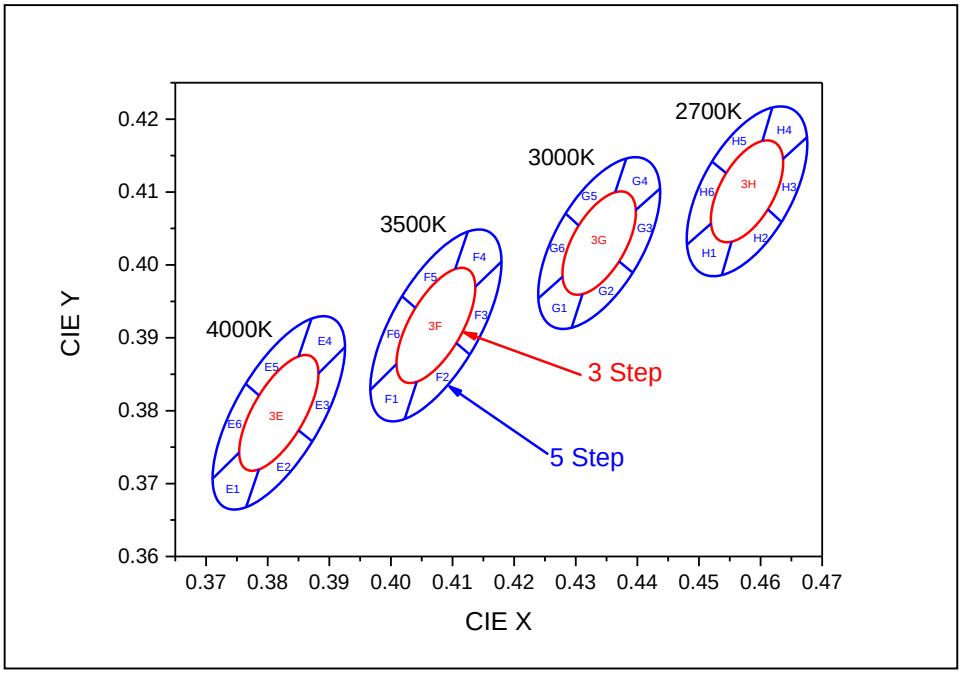


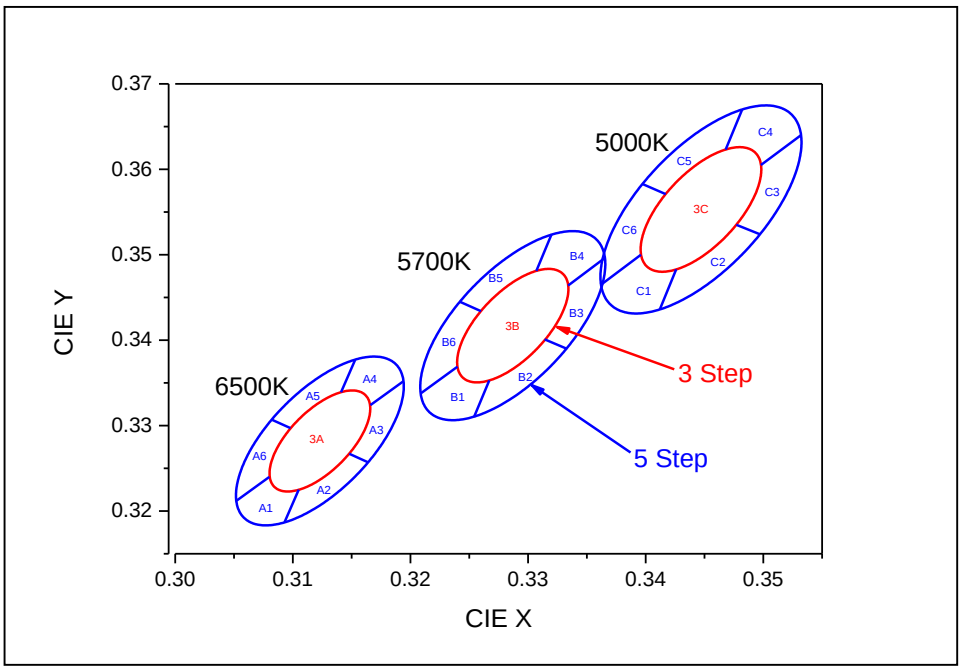
[Binning Information]

	Bin #1	Bin #2
VF	Y2	Y2
	Y3	Y3
	Z1	Z1
	Z2	Z2
	Z3	Z3
CIE	3S bin	3S bin
	1 bin	4 bin
	2 bin	5 bin
	3 bin	6 bin

Color Bin Structure

CIE Chromaticity Diagram T_a=25℃, I_F=150mA



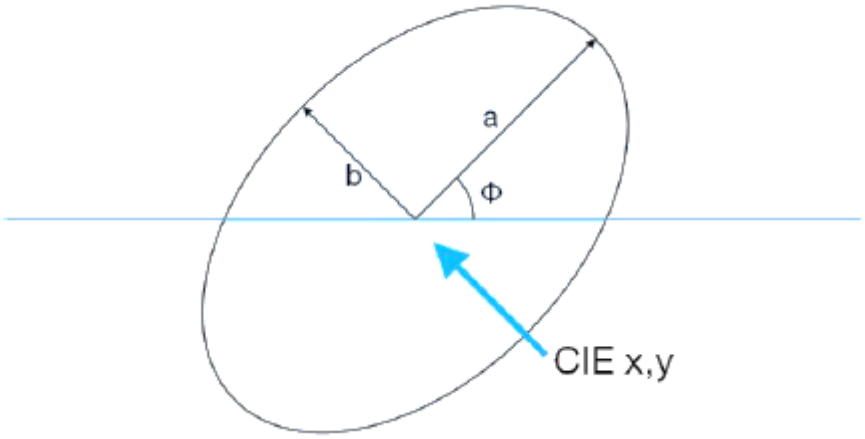


***Notes :**

1. H=2700K G=3000K F=3500K E=4000K C=5000K B=5700K A=6500K

Color Bin Structure

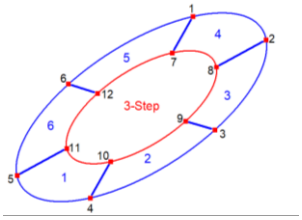
Chromaticity Region & Coordinates



MacAdam	CCT (K)	Center point		Major-axis	Minor-axis	Rotation
		CIE x	CIE y	a	b	Φ
3S	2700	0.4578	0.4101	0.0081	0.0042	53.7
	3000	0.4338	0.403	0.0083	0.0041	53.22
	3500	0.4073	0.3917	0.0093	0.0041	54
	4000	0.3818	0.3797	0.0094	0.004	53.72
	5000	0.3447	0.3553	0.0082	0.0035	59.62
	5700	0.3287	0.3417	0.0075	0.0032	59.1
	6500	0.3123	0.3282	0.0067	0.0029	58.57
5S	2700	0.4578	0.4101	0.0135	0.007	53.7
	3000	0.4338	0.403	0.0138	0.0068	53.22
	3500	0.4073	0.3917	0.0155	0.0068	54
	4000	0.3818	0.3797	0.0157	0.0067	53.72
	5000	0.3447	0.3553	0.0137	0.0058	59.62
	5700	0.3287	0.3417	0.0125	0.0053	59.1
	6500	0.3123	0.3282	0.0112	0.0048	58.57

Color Bin Structure

Chromaticity Region & Coordinates



CCT	Region	CIE x	CIE y	CCT	Region	CIE x	CIE y	CCT	Region	CIE x	CIE y
2700K	1	0.4521	0.4142	3000K	1	0.4283	0.4071	3500K	1	0.4018	0.3957
	2	0.4619	0.4216		2	0.4382	0.4146		2	0.4125	0.4046
	3	0.4675	0.4175		3	0.4437	0.4105		3	0.418	0.4005
	4	0.4634	0.4059		4	0.4393	0.3989		4	0.4128	0.3877
	5	0.4537	0.3986		5	0.4293	0.3913		5	0.4022	0.3788
	6	0.4481	0.4028		6	0.4239	0.3954		6	0.3966	0.3828
	7	0.4544	0.4126		7	0.4305	0.4054		7	0.404	0.3941
	8	0.4603	0.417		8	0.4364	0.41		8	0.4104	0.3994
	9	0.4636	0.4145		9	0.4397	0.4075		9	0.4137	0.397
	10	0.4612	0.4076		10	0.437	0.4005		10	0.4106	0.3893
	11	0.4553	0.4032		11	0.4311	0.396		11	0.4042	0.384
	12	0.452	0.4057		12	0.4279	0.3984		12	0.4009	0.3864
4000K	1	0.3764	0.3837	5000K	1	0.3397	0.3583	5700K	1	0.3242	0.3445
	2	0.3871	0.3926		2	0.3482	0.367		2	0.332	0.3524
	3	0.3925	0.3887		3	0.3532	0.364		3	0.3365	0.3496
	4	0.3872	0.3758		4	0.3497	0.3524		4	0.3333	0.339
	5	0.3765	0.3668		5	0.3412	0.3436		5	0.3254	0.331
	6	0.3711	0.3707		6	0.3362	0.3465		6	0.3209	0.3338
	7	0.3786	0.3821		7	0.3417	0.3571		7	0.326	0.3434
	8	0.385	0.3874		8	0.3468	0.3623		8	0.3307	0.3481
	9	0.3882	0.3851		9	0.3498	0.3605		9	0.3334	0.3464
	10	0.385	0.3773		10	0.3477	0.3535		10	0.3314	0.3401
	11	0.3786	0.372		11	0.3426	0.3483		11	0.3267	0.3353
	12	0.3754	0.3743		12	0.3396	0.35		12	0.324	0.3369

***Notes :**

1. H=2700K G=3000K F=3500K E=4000K C=5000K B=5700K A=6500K

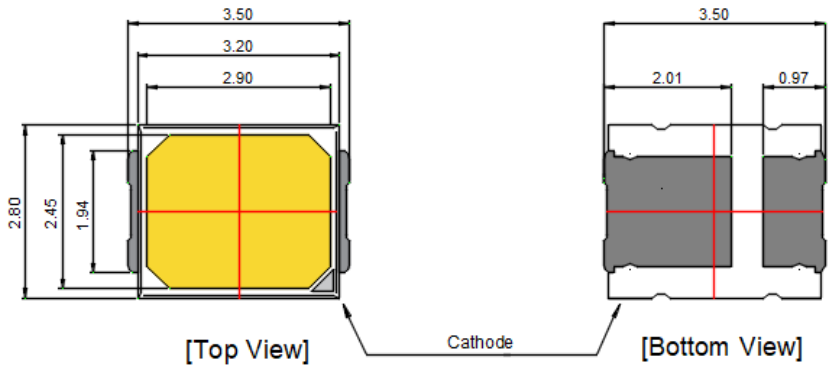
Color Bin Structure

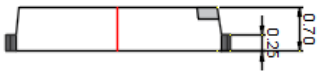
Chromaticity Region & Coordinates

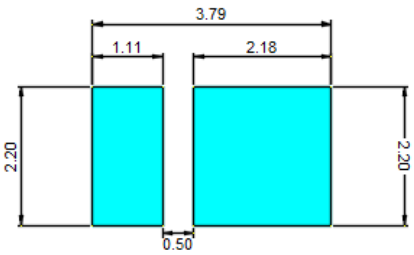
CCT	Region	CIE x	CIE y
6500K	1	0. 3082	0. 3307
	2	0. 3153	0. 3377
	3	0. 3194	0. 3352
	4	0. 3164	0. 3257
	5	0. 3093	0. 3187
	6	0. 3052	0. 3212
	7	0. 3098	0. 3297
	8	0. 3141	0. 3339
	9	0. 3166	0. 3324
	10	0. 3148	0. 3267
	11	0. 3105	0. 3225
	12	0. 308	0. 324

***Notes :**
1. H=2700K G=3000K F=3500K E=4000K C=5000K B=5700K A=6500K

Mechanical Dimensions





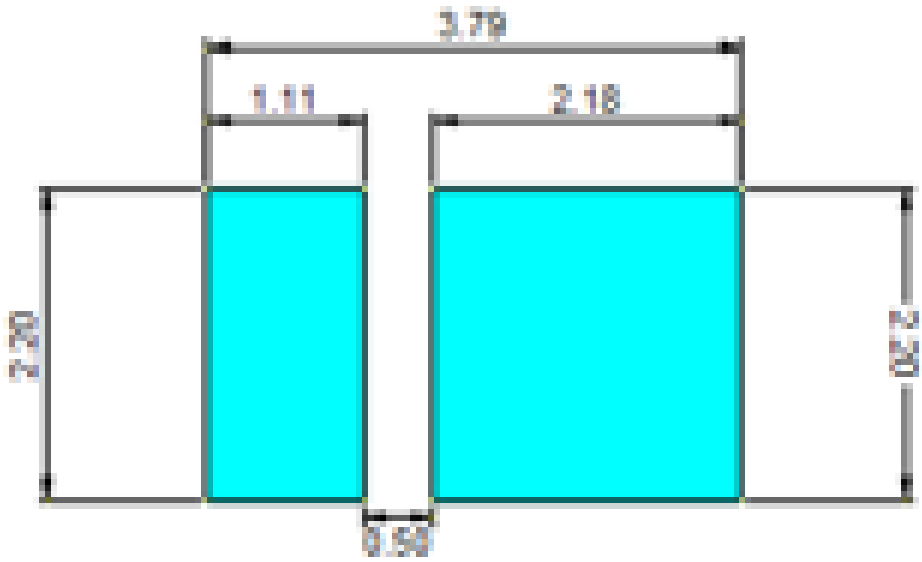


[RECOMMENDED PCB SOLDER PAD]

Notes :

(1) All dimensions are in millimeters.
(2) Scale : none
(3) Undefined tolerance is ±0.2mm

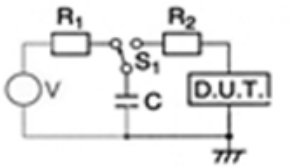
Recommended Solder Pad



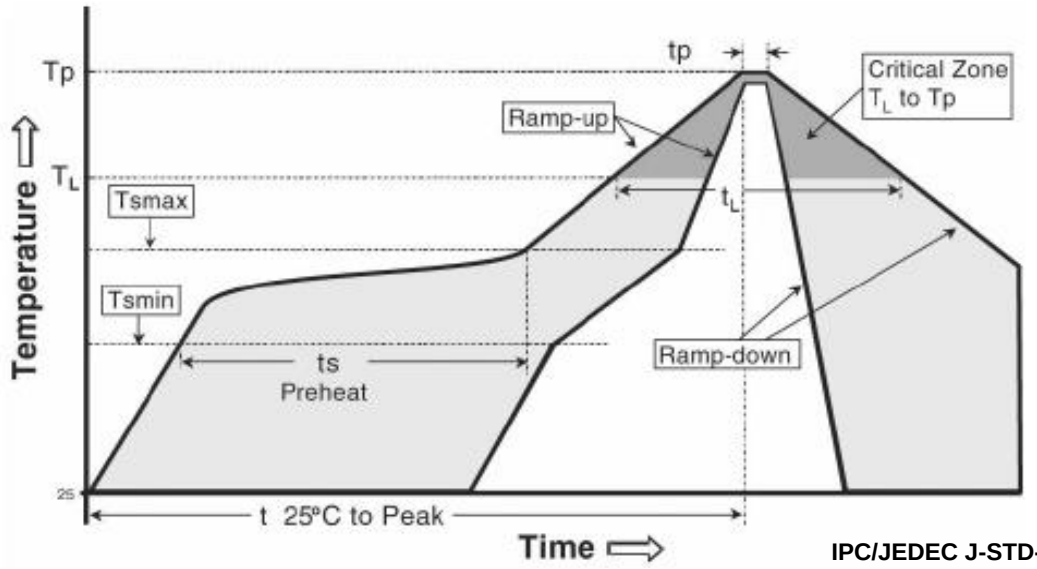
Note:

(1) All dimensions are in millimeters.
(2) Scale : none
(3) This drawing without tolerances are for reference only
(4) Undefined tolerance is ±0.1mm
(5) The appearance and specifications of the product may be changed for improvement without notice.

Reliability Test Item & Condition

Test Item	Test Condition	Test Hour / Cycle	Sample No.
Room Temperature Life Test	DC Max current	1000 h	22
High Temperature Life Test	85 ºC, DC Max current	1000 h	22
High Temperature Humidity Life Test	60 ºC, 90 % RH, DC Max current	1000 h	22
Low Temperature Life Test	-40 ºC, DC Max current	1000 h	22
Powered Temperature Cycle Test	-45 ºC ~ 85 ºC, each 20 min, on/off 5 min Temp. Change time 100min, DC Max current	100 cycles	22
Temperature Cycling	-45 ºC / 15 min ↔ 125 ºC / 15 min	200 cycles	100
High Temperature Storage	85 ºC	1000 h	11
Low Temperature Storage	-40 ºC	1000 h	11
ESD (HBM)	 R_1: 10 MΩ R_2: 1.5 kΩ C: 100 pF V: ±2 kV	5 times	30

Reflow Soldering Characteristics



IPC/JEDEC J-STD-020

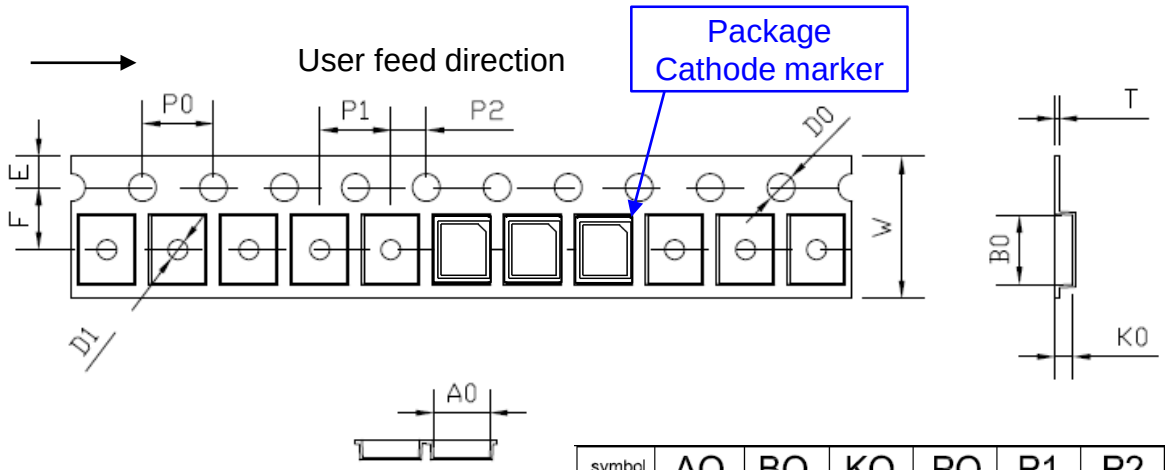
Table 7.

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_{smax} to T_p)	3° C/second max.	3° C/second max.
Preheat - Temperature Min (T_{smin}) - Temperature Max (T_{smax}) - Time (T_{smin} to T_{smax}) (t_s)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	 183 °C 60-150 seconds	 217 °C 60-150 seconds
Peak Temperature (T_p)	215℃	260℃
Time within 5°C of actual Peak Temperature (t_p)2	10-30 seconds	20-40 seconds
Ramp-down Rate	6 °C/second max.	6 °C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

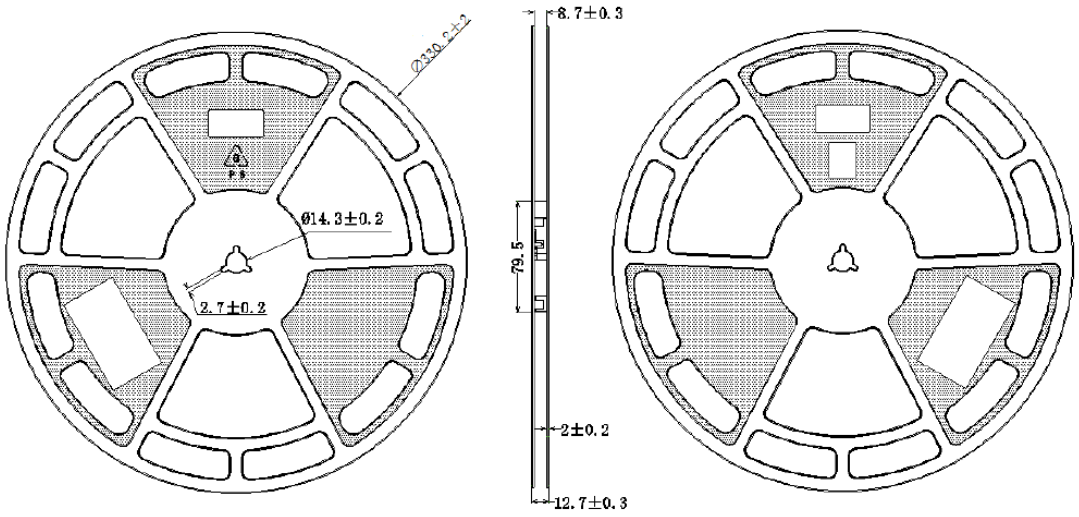
Caution

(1) Reflow soldering is recommended not to be done more than two times. In the case of more than 24 hours passed soldering after first, LEDs will be damaged.
(2) Repairs should not be done after the LEDs have been soldered. When repair is unavoidable, suitable tools must be used.
(3) Die slug is to be soldered.
(4) When soldering, do not put stress on the LEDs during heating.
(5) After soldering, do not warp the circuit board.

Emitter Tape & Reel Packaging



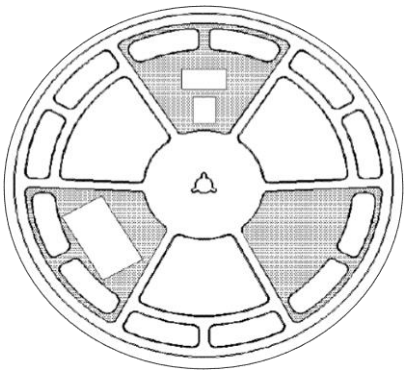
symbol	AO	BO	KO	PO	P1	P2
Spec	3.0±0.10	3.75±0.15	1.05±0.15	4.0±0.10	4.0±0.10	2.0±0.10
symbol	W	T	E	F	DO	D1
Spec	8.00±0.10	0.20±0.05	1.75±0.10	3.5±0.10	1.5±0.05	1.10±0.10



Notes :

(1) Quantity : Max 16,000pcs/Reel
(2) Cumulative Tolerance : Cumulative Tolerance/10 pitches to be ±0.2mm
(3) Adhesion Strength of Cover Tape
Adhesion strength to be 0.1-0.7N when the cover tape is turned off from the carrier tape at the angle of 10˚ to the carrier tape.
(4) Package : P/N, Manufacturing data Code No. and Quantity to be indicated on a damp proof Package.

Emitter Tape & Reel Packaging



Humidity Indicator

Desiccant

Label

RANK : $Z_1Z_1Z_1Z_2Z_2Z_3Z_3Z_3$

QUANTITY : 16000

LOT : $Y_1Y_2Y_3Y_4Y_5Y_6Y_7Y_8Y_9Y_{10}$ – $Y_{11}Y_{12}Y_{13}Y_{14}Y_{15}Y_{16}Y_{17}$

SSC PART NUMBER : $X_1X_2X_3X_4X_5X_6X_7X_8$-X_9X_{10}

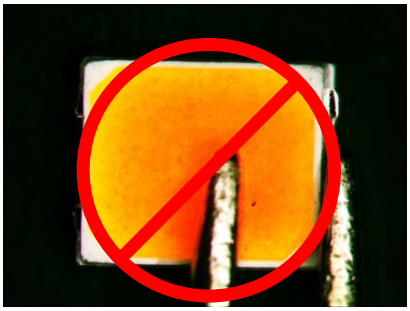
ULB

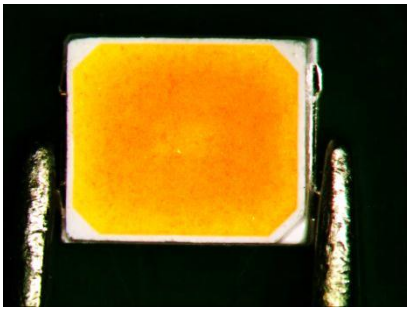
Notes :

(1) Rank : Flux: $Z_1Z_1Z_1$,CIE: Z_2Z_2, VF: $Z_3Z_3Z_3$
(2) Quantity : Max 16,000pcs/Reel
(3) Lot no.: $Y_1Y_2Y_3Y_4Y_5Y_6Y_7Y_8Y_9Y_{10}$ – SSC 18digit code
(4) SSC part Number : $X_1X_2X_3X_4X_5X_6X_7X_8$-X_9X_{10}

Handling of Silicone Resin for LEDs

(1) During processing, mechanical stress on the surface should be minimized as much as possible. Sharp objects of all types should not be used to pierce the sealing compound.





(2) In general, LEDs should only be handled from the side. By the way, this also applies to LEDs without a silicone sealant, since the surface can also become scratched.

(3) When populating boards in SMT production, there are basically no restrictions regarding the form of the pick and place nozzle, except that mechanical pressure on the surface of the resin must be prevented. This is assured by choosing a pick and place nozzle which is larger than the LED's reflector area.

(4) Silicone differs from materials conventionally used for the manufacturing of LEDs. These conditions must be considered during the handling of such devices. Compared to standard encapsulants, silicone is generally softer, and the surface is more likely to attract dust.

As mentioned previously, the increased sensitivity to dust requires special care during processing. In cases where a minimal level of dirt and dust particles cannot be guaranteed, a suitable cleaning solution must be applied to the surface after the soldering of components.

(5) SSC suggests using isopropyl alcohol for cleaning. In case other solvents are used, it must be assured that these solvents do not dissolve the package or resin.
Ultrasonic cleaning is not recommended. Ultrasonic cleaning may cause damage to the LED.

(6) Please do not mold this product into another resin (epoxy, urethane, etc) and do not handle this. product with acid or sulfur material in sealed space.

Precaution for Use

(1) Storage

To avoid the moisture penetration, we recommend store in a dry box with a desiccant.

The maximum storage temperature range is 40℃ and a maximum humidity of RH90%.

(2) Use Precaution after Opening the Packaging

Use SMT techniques properly when the LED is to be soldered dipped as separation of the lens may affect the light output efficiency.

Pay attention to the following:

a. Recommend conditions after opening the package

- Sealing
- Temperature : 30℃ Humidity : less than RH60%

b. If the package has been opened more than 4 week(MSL_2a) or the color of the desiccant changes, components should be dried for 10-24hr at 65±5℃

(3) Do not apply mechanical force or excess vibration during the cooling process to normal temperature after soldering.

(4) Do not rapidly cool device after soldering.

(5) Components should not be mounted on warped (non coplanar) portion of PCB.

(6) Radioactive exposure is not considered for the products listed here in.

(7) Gallium arsenide is used in some of the products listed in this publication.

These products are dangerous if they are burned or shredded in the process of disposal. It is also dangerous to drink the liquid or inhale the gas generated by such products when chemically disposed of.

(8) This device should not be used in any type of fluid such as water, oil, organic solvent and etc.

When washing is required, IPA (Isopropyl Alcohol) should be used.

(9) When the LEDs are in operation the maximum current should be decided after measuring the package temperature.

Precaution for Use

(10) The appearance and specifications of the product may be modified for improvement without notice.

(11) Long time exposure of sunlight or occasional UV exposure will cause lens discoloration.

(12) VOCs (Volatile organic compounds) emitted from materials used in the construction of fixtures can penetrate silicone encapsulants of LEDs and discolor when exposed to heat and photonic energy. The result can be a significant loss of light output from the fixture. Knowledge of the properties of the materials selected to be used in the construction of fixtures can help prevent these issues.

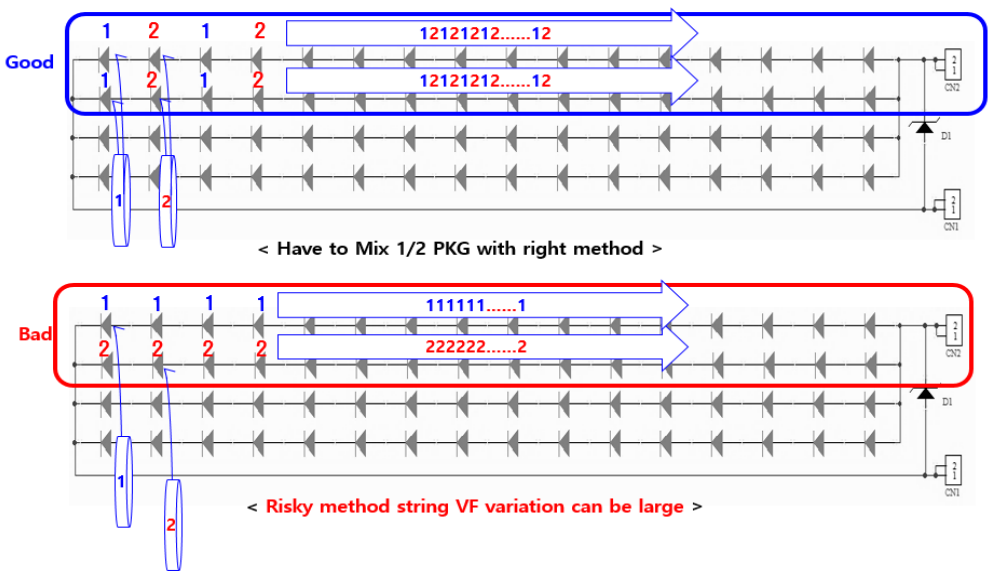
(13) Attaching LEDs, do not use adhesives that outgas organic vapor.

(14) The driving circuit must be designed to allow forward voltage only when it is ON or OFF.
If the reverse voltage is applied to LED, migration can be generated resulting in LED damage.

(15) Similar to most Solid state devices;
LEDs are sensitive to Electro-Static Discharge (ESD) and Electrical Over Stress (EOS).
Below is a list of suggestions that Seoul Semiconductor purposes to minimize these effects.

(16) Voltage Variation Mixing

If Module circuit series and parallel many PKG, voltage variation problem coming out seriously.
To avoid this issue we recommend mixing Vf bin at the SMD Module Program level. Even though using Single bin only.
For example, when configuring a module with two reels (reel1 and Reel2), SMT should be as follows Good below.



Precaution for Use

a. ESD (Electro Static Discharge)

Electrostatic discharge (ESD) is the defined as the release of static electricity when two objects come into contact. While most ESD events are considered harmless, it can be an expensive problem in many industrial environments during production and storage. The damage from ESD to an LEDs may cause the product to demonstrate unusual characteristics such as:

- Increase in reverse leakage current lowered turn-on voltage
- Abnormal emissions from the LED at low current

The following recommendations are suggested to help minimize the potential for an ESD event.
One or more recommended work area suggestions:

- Ionizing fan setup
- ESD table/shelf mat made of conductive materials
- ESD safe storage containers

One or more personnel suggestion options:

- Antistatic wrist-strap
- Antistatic material shoes
- Antistatic clothes

Environmental controls:

- Humidity control (ESD gets worse in a dry environment)

b. EOS (Electrical Over Stress)

Electrical Over-Stress (EOS) is defined as damage that may occur when an electronic device is subjected to a current or voltage that is beyond the maximum specification limits of the device.
The effects from an EOS event can be noticed through product performance like:

- Changes to the performance of the LED package
  (If the damage is around the bond pad area and since the package is completely encapsulated the package may turn on but flicker show severe performance degradation.)
- Changes to the light output of the luminaire from component failure
- Components on the board not operating at determined drive power

Failure of performance from entire fixture due to changes in circuit voltage and current across total circuit causing trickle down failures. It is impossible to predict the failure mode of every LED exposed to electrical overstress as the failure modes have been investigated to vary, but there are some common signs that will indicate an EOS event has occurred:

- Damaged may be noticed to the bond wires (appearing similar to a blown fuse)
- Damage to the bond pads located on the emission surface of the LED package
  (shadowing can be noticed around the bond pads while viewing through a microscope)
- Anomalies noticed in the encapsulation and phosphor around the bond wires.
- This damage usually appears due to the thermal stress produced during the EOS event.

c. To help minimize the damage from an EOS event Seoul Semiconductor recommends utilizing:

- A surge protection circuit
- An appropriately rated over voltage protection device
- A current limiting device

Company Information

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Seoul Semiconductor (www.SeoulSemicon.com) manufacturers and packages a wide selection of light emitting diodes (LEDs) for the automotive, general illumination/lighting, Home appliance, signage and back lighting markets. The company is the world's fifth largest LED supplier, holding more than 10,000 patents globally, while offering a wide range of LED technology and production capacity in areas such as "nPola", "Acrich", the world's first commercially produced AC LED, and "Acrich MJT - Multi-Junction Technology" a proprietary family of high-voltage LEDs.

The company's broad product portfolio includes a wide array of package and device choices such as Acrich and Acirch2, high-brightness LEDs, mid-power LEDs, side-view LEDs, and through-hole type LEDs as well as custom modules, displays, and sensors.

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